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EXAMINER	
YANG, LINA	
ART UNIT	**PAPER NUMBER**
2665	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,835	YUN ET AL.	
	Examiner	Art Unit	
	Lina Yang	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,25,26,28,36-56 and 63-65* is/are rejected.

7)☒ Claim(s) *21-24,27,29-35,57-61,64 and 66-71* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/24/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351 (a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 36-37, are rejected under 35 U.S.C. 102(e) as being anticipated by Chao (U.S. Patent No. 6,487,213 B1).

Regarding claim 36, Chao teaches a hierarchical arbitration method comprising (sections 2.2.3 and 5.1.1):

for each switch output, arbitrating between a plurality of available switch inputs (section 2.2.3 and 5.1.1 ; col. 8 lines 21-56 and col. 13 lines 44-48);

arbitrating between the contending switch outputs (section 2.2.3 and 5.1.1 ; col. 8 lines 21-56 and col. 13 lines 44-48);

arbitrating between available switch inputs, and between nominating switch outputs for each of a plurality of crossbars (section 2.2.3 and 5.1.1 ; col. 8 lines 21-56 and col. 13 lines 44-48), and,

arbitrating for each crossbar in a plurality of arbitration cycles (section 2.2.3 and 5.1.1 ; col. 8 lines 21-56 and col. 13 lines 44-48).

Regarding claim 37, Chao further teaches that following arbitration between contending switch outputs, accepting a switch output for linkage to a switch input; and, in response to accepting a switch output, selecting a switch input queue (col. 14 lines 2-12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 20, 25 and 38are rejected under 35 U.S.C. 103(a) as being unpatentable over by Chao (U. S. Patent No. 6,487,213 B1) in view of Salandro (U. S. Patent No. 6,519,540 B1).

Regarding claim 1, Chao teaches a hierarchical arbitration method in a switch system comprising:

accepting variably sized information packets including a plurality of cells at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs (col. 8 lines 21-24 and 27-33; fig. 19 and 20);

at each switch input, queuing the information packets into a plurality of queues col. 8 lines 59-67) ;

simultaneously arbitrating for a plurality of links between switch inputs and switch outputs (col. 19 lines 47-49); and,

transferring information packets across the links (col. 8 lines 39-46).

Chao differs from the claimed invention in that Chao does not specifically teach locking the links. However, Salandro teaches that the switch locks the links (col. 7 lines 11-15). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the switch locks the links, as taught by Salandro in the assembly of Chao in order to prevent others from changing the signal path or establishing a signal path through the switch.

Regarding claim 2, Chao further teaches that parsing the information packets into units of one cell (col. 8 lines 27-33); and,

wherein transferring the information packets includes transferring the information packets in units of one cell per master decision cycle ("time slot") (col. 8 lines 39-46 and col. 11 lines 49-53).

Regarding claim 3, Chao further teaches that for each linked switch input, selecting a queue (col. 8 lines 66-67).

Regarding claim 4, Chao teaches a hierarchical arbitration method in a switch system comprising:

accepting variably sized information packets including a plurality of cells, at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs (col. 8 lines 21-24 and 27-33; fig. 19 and 20);

parsing the information packets into units of one cell (col. 8 lines 27-33);

simultaneously arbitrating for a link to each switch output, from each switch input (col. 19 lines 47-49);

for each linked switch input, selecting a queue (col. 8 lines 66-67); and,

transferring information packets across the links in units of one cell per master decision cycle ("time slot") (col. 8 lines 39-46 and col. 11 lines 49-53).

Chao differs from the claimed invention in that Chao does not specifically teach locking the links. However, Salandro teaches that the switch locks the links (col. 7 lines 11-15). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links, as taught by Salandro in the assembly of Chao in order to prevent others from changing the signal path or establishing a signal path through the switch.

Regarding claim 5, Chao further teaches that a first plurality of crossbars are included with a plurality of parallel routed switch inputs and a plurality of parallel routed switch outputs (fig. 20); and, the method further comprising:
arbitrating for a link to each switch output, for each of the first plurality of crossbars (fig. 19 and 20; col. 8 lines 47-53 and col. 19 lines 47-49).

Regarding claim 6, Chao further teaches that arbitrating for a link to each switch output, for each of the first plurality of crossbars includes arbitrating for up to a first plurality of links to each switch output, per master decision cycle ("time slot") (fig. 19 and 20; col. 8 lines 39-53; col. 11 lines 49-53 and col. 19 lines 47-49).

Regarding claim 7, Chao further teaches that arbitrating for up to a first plurality to each switch output includes, for each crossbar, includes:
simultaneously arbitrating between a plurality of available switch inputs having information packets addressed to a switch output (col. 8 lines 39-46)

Regarding claim 20, Chao teaches that in a switch system including a first plurality of crossbars with a plurality of parallel routed switch inputs and a plurality of parallel routed switch outputs, a hierarchical arbitration method comprising:

accepting variably sized information packets including a plurality of cells, at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs (col. 8 lines 21-24 and 27-33; fig. 19 and 20);

simultaneously arbitrating for a plurality of links between switch inputs and switch outputs in a plurality of arbitration cycles for each crossbar, where each switch output in a crossbar simultaneously nominates an available switch input (col. 14 lines 2-12 and col. 19 lines 47-49); and,

transferring information packets across the links (col. 8 lines 39-46).

Chao differs from the claimed invention in that Chao does not specifically teach locking the links. However, Salandro teaches that the switch locks the links (col. 7 lines 11-15). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the switch locks the links, as taught by Salandro in the assembly of Chao in order to prevent others from changing the signal path or establishing a signal path through the switch.

Regarding claim 25, Chao teaches that in a n a switch system including a first plurality of crossbars with a plurality of parallel routed switch inputs and a plurality of parallel routed switch outputs, a hierarchical arbitration method comprising:

accepting variably sized information packets including a plurality of cells at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs (col. 8 lines 21-24 and 27-33; fig. 19 and 20);

at each switch input, queuing the information packets into a plurality of queues(col. 8 lines 59-67) ;

simultaneously arbitrating for a plurality links between switch inputs and switch outputs (col. 19 lines 47-49);

selecting a queue for each locked link, for each crossbar (col. 14 lines 2-12); and transferring information packets across the links (col. 8 lines 39-46).

Chao differs from the claimed invention in that Chao does not specifically teach locking the links. However, Salandro teaches that the switch locks the links (col. 7 lines 11-15). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the switch locks the links, as taught by Salandro in the assembly of Chao in order to prevent others from changing the signal path or establishing a signal path through the switch.

Regarding claim 38, Chao teaches a hierarchical arbitration system for transferring information across a switch, the system comprising (fig. 20; col. 21 lines 60-67 and col. 22 lines 1-2):

a switch having a plurality of inputs (fig. 20, 256 inputs), a control input to accept arbitration commands (see output lines from the AR16 to each SW16 in fig. 20) , and a plurality of outputs selectively connected to the switch inputs in response to the arbitration commands (inherent to a crossbar switch; the connections are set according to the arbitration commands);

an arbiter having an output connected to the switch control input to supply simultaneously arbitrated link commands for a plurality of links between the switch inputs and the switch outputs (AR16 in fig. 20); and,

in response to commands from the arbiter, to transfer variably sized information packets across the links (col. 8 lines 39-46).

Chao differs from the claimed invention in that Chao does not specifically teach that the switch locks the links locking between switch inputs and switch outputs. However, Salandro teaches that the switch locks the links between switch inputs and switch outputs (col. 7 lines 11-15). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the switch locks the links between switch inputs and switch outputs, as taught by Salandro in the assembly of Chao in order to prevent others from changing the signal path or establishing a signal path through the switch.

3. Claims 8-11, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Chao (U. S. Patent No. 6,487,213 B1) in view of Krishna et al. (U. S. Patent Application No. 20010050916 A1).

Regarding claim 8, Chao differs from the claimed invention in that Chao does not specifically teach that the arbitrating between a plurality of available switch inputs includes selecting the least recently available switch input. However, Krishna teaches the arbitrating between a plurality of available switch inputs includes selecting the least

recently available switch input ([0124] and TABLE 1 "picks the requesting input port with the oldest time stamp set along with the request"). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the arbitrating between a plurality of available switch inputs includes selecting the least recently available switch input, as taught by Krishna in the assembly of Chao in order to arbitrate effectively which input ports receives the grant from the output port.

Regarding claim 9, Chao further teaches that the arbitrating between a plurality of available switch inputs includes arbitrating in a plurality of arbitration cycles for each crossbar (col. 14 lines 2-12).

Regarding claim 10, Chao teaches that in a switch system including a first plurality of crossbars with a plurality of parallel routed switch inputs and a plurality of parallel routed switch outputs, a hierarchical arbitration method comprising:

accepting variably sized information packets including a plurality of cells, at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs (col. 8 lines 21-24 and 27-33; fig. 19 and 20);

parsing the information packets into units of one cell (col. 8 lines 27-33);

arbitrating for up to a first plurality of links to each switch output from a plurality of available switch inputs having information packets addressed to that switch output, per master decision cycle ("time slot") (fig. 19 and 20; col. 8 lines 39-53; col. 11 lines 49-53 and col. 19 lines 47-49) as follows:

establishing an available switch input priority list for each switch output (col. 14 section 5.1.2 and fig. 9 and fig. 10);

nominating switch inputs in response to the available switch input priority (col. 14 section 5.1.2 and fig. 9 and fig. 10);

arbitrating for links to each switch output, for each of the first plurality of crossbars (fig. 19 and fig. 20; col. 8 lines 39-53; col. 11 lines 49-53 and col. 19 lines 47-49);

arbitrating in a plurality of arbitration cycles for each crossbar (col. 14 lines 2-12);

locking the links (col. 8 lines 39-46); and,

transferring information packets across the links in units of one cell per master decision cycle ("time slot") (col. 8 lines 39-46 and col. 11 lines 49-53).

Chao differs from the claimed invention in that Chao does not specifically teach that the arbitrating between a plurality of available switch inputs includes selecting the least recently available switch input. However, Krishna teaches the arbitrating between a plurality of available switch inputs includes selecting the least recently available switch input ([0124] and TABLE 1 "picks the requesting input port with the oldest time stamp set along with the request"). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the arbitrating between a plurality of available switch inputs includes selecting the least recently available switch input, as taught by Krishna in the assembly of Chao in order to arbitrate effectively which input ports receives the grant from the output port.

Regarding claim 11, Chao further teaches that arbitrating in a plurality of arbitration cycles for each crossbar includes:

for each switch output, nominating the highest priority available switch input in a first arbitration cycle (col. 14 lines 2-12); and,

if the nominating switch output is not accepted, nominating successively lower priority available switch inputs in subsequent arbitration cycles (fig. 10 and fig. 11; col. 14 lines 2-12).

Regarding claim 26, Chao differs from the claimed invention in that Chao does not specifically teach that selecting a queue for each locked link, for each crossbar, includes selecting the least recently available queue. However, Krishna teaches selecting a queue for each locked link, for each crossbar, includes selecting the least recently available queue ([0124] and TABLE 1 "picks the requesting input port with the oldest time stamp set along with the request"). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include selecting a queue for each locked link, for each crossbar, includes selecting the least recently available queue, as taught by Krishna in the assembly of Chao in order to have effectively switch throughput

4. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Angle et al. (U. S. Patent Application No. 20030174701 A1) in view of Chao (U. S. Patent No. 6,487,213 B1.

Regarding claim 17, Angle teaches in a switch system including a first plurality of crossbars with a plurality of parallel routed switch inputs and a plurality of parallel routed switch outputs, a hierarchical arbitration method comprising:

accepting packets including a plurality of cells, at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs ([0032]);

parsing the information packets into units of one cell ([0032]);

arbitrating for up to a first plurality of links to each switch output from a plurality of available switch inputs having information packets addressed to that switch output, per master decision cycle as follows:

establishing an available switch input priority list, with a sequential pointer, for each switch output ("priority indicator" for input ports in each out port in fig. 7A; and [0081]); and,

nominating switch inputs in response to the available switch input priority list ([0081]);

arbitrating for links to each switch output, for each of the first plurality of crossbars in a corresponding first plurality of minor decision cycles ("cell cycle"; [0008]);

arbitrating in a plurality of arbitration cycles each minor decision cycle as follows:

for each switch output, nominating the highest priority available switch input in a first arbitration cycle (fig. 7A and [0081]);

for each switch input receiving multiple nominations, simultaneously accepting the least recently available nominating switch output as follows:

for each available switch input, establishing a nominating switch output priority list ("priority indicator" for output ports in each input port in fig. 7B; and [0085]); and,

accepting nominating switch outputs in response to the nominating switch output priority list (fig. 7B; [0085] and [0086]); and,

if the nominating switch output is not accepted, nominating successively lower priority available switch inputs in subsequent arbitration cycles (fig. 7B; and [0085] and [0086]);

locking the links ([0042]) ;

transferring information packets across the links in units of one cell per master decision cycle ([0042]) ;

advancing each input pointer to an input next in sequence to the selected switch input, if the selection occurs in a first arbitration cycle (fig. 7A and [0081]); and,

nominating the available switch input closest in succession to the second switch input in subsequent arbitrations (fig. 7A and [0081]).

Angle differs from the claimed invention in that Angle does not specifically teach that the packets are variably sized information packets including a plurality of cells, at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs. However, Chao teaches that the packets can be variable sized (col. 8 lines 21-24 and 27-33; fig. 19 and 20). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include accepting variably sized information packets, as taught by Chao in the assembly of Angle in order to accommodate different data packets.

Regarding claim 18, Angle further teaches that accepting nominating switch outputs in response to the nominating switch output priority list includes limiting the nominating output arbitration process to a single arbitration cycle (fig. 6 step 630 and [0086]).

Regarding claim 19, Angle further teaches that establishing a nominating switch output priority list includes creating a sequential output pointer for each nominating switch output priority list (fig. 7B; and [0085]); and, the method further comprising:

following the acceptance of a nominating switch output in a first arbitration cycle, advancing the pointer to a suggested switch output, next in sequence to the selected switch output (fig. 6 step 650); and,

accepting the nominating switch output closest in succession to the suggested switch output in subsequent arbitrations (fig. 6 step 650; fig. 7B; and [0085]).

5. Claim 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Chao (U. S. Patent No. 6,487,213 B1) in view of Fan et al. (U. S. Patent Application No. 20020122428 A1).

Regarding claim 28, Chao further teaches that at a plurality of switch inputs, includes accepting information packets having a ranked class of service (COS) (section 2.2.2 col. 7 lines 57-67 and col. 8 lines 1-18; section 5.1.6 col. 16 lines 52-57). Chao differs from the claimed invention in that Chao does not specifically teach that queuing

information packets into a plurality of queues includes queuing the information packets by COS and selecting a queue includes each nominated switch input selecting a queue in response to COS of the information packets available for each crossbar. However, Fan teaches queuing information packets into a plurality of queues includes queuing the information packets by COS; and, wherein selecting a queue includes each nominated switch input selecting a queue in response to COS of the information packets available for each crossbar ([0043] and [0045]). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include queuing information packets into a plurality of queues includes queuing the information packets by COS and selecting a queue includes each nominated switch input selecting a queue in response to COS of the information packets available for each crossbar, as taught by Fan in the assembly of Chao in order to provide queuing structure for class Quality of Service (QoS).

6. Claims 39-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Chao (U. S. Patent No. 6,487,213 B1) in view of Alasti et al. (U. S. Patent Application No. 20030072326 A1).

Regarding claim 39, Chao further teaches the system accepting variably sized information packets including a plurality of cells at a plurality of switch inputs, the plurality of information packets addressing a plurality of switch outputs (col. 8 lines 21-24 and 27-33; fig. 19 and 20) and a control input to accept queue selection commands (fig. 20 outgoing lines from the AR 16). Chao differs from the claimed invention in that

Chao does not specifically teach the system further comprising: the queue assembler grouping the information packets by switch output address, queuing the information packets into a plurality of queues for each address grouping, and supplying queues, selected in response to queue selection commands, at a plurality of outputs connected to corresponding switch inputs. However, Alasti teaches that the system further comprising: the queue assembler grouping the information packets by switch output address (fig. 1 and [0025]), queuing the information packets into a plurality of queues for each address grouping (121 in fig. 1 and [0025]), and supplying queues, selected in response to queue selection commands (the output lines from "scheduler in fig. 1), at a plurality of outputs connected to corresponding switch inputs (fig.1 and fig. 2).

Regarding claim 40, Chao further teaches that teaches the queue assembler parses the information packets into units of one cell (col. 8 lines 27-33); and, wherein the switch transfers the information packets in units of one cell per master decision cycle ("time slot") (col. 8 lines 39-46 and col. 11 lines 49-53).

Regarding claim 41, Alasti further teaches that the arbiter has an output connected to the control input of the queue assembler to select a queue for each linked switch input (fig. 1 and fig. 2).

Regarding claim 42, Alasti further teaches that the arbiter simultaneously arbitrates a link for each switch output (fig. 1 and fig. 2).

7. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Chao (U. S. Patent No. 6,487,213 B1) in view of Krishna et al. (U. S. Patent Application No. 20010050916 A1) as applied to claim 11 above, and further in view of Angle et al. (U. S. Patent Application No. 20030174701 A1).

Regarding claim 12, the modified assembly of Chao and Krishna differs from the claimed invention in that the modified assembly does not specifically teach that for each switch input receiving multiple nominations, arbitrating between the nominating switch outputs. However, Angle teaches for each switch input receiving multiple nominations, arbitrating between the nominating switch outputs (fig. 7B and [0085]). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include for each switch input receiving multiple nominations, arbitrating between the nominating switch outputs, as taught by angle in the modified assembly of Chao and Krishna in order to solve the contention for input ports.

Regarding claim 13, Angle further teaches that arbitrating between the nominating switch outputs includes accepting the least recently available nominating switch output (fig. 7B and [0085]).

Regarding claim 14, Angle further teaches that accepting the least recently nominating switch output includes: for each available switch input, establishing a

nominating switch output priority list (fig. 7B); and, accepting nominating switch outputs in response to the nominating switch output priority list (fig. 7B and [0085]).

Regarding claim 15, Angle further teaches that arbitrating between nominating switch outputs includes the arbitrating switch inputs simultaneously accepting nominating switch outputs (fig. 7B and [0085]).

Regarding claim 16, Angle further teaches that arbitrating for links to each switch output, for each of the first plurality of crossbars includes arbitrating for each of the first plurality of crossbars in a corresponding first plurality of minor decision cycles ("cell cycle"; [0008]).

8. Claims 43-44, 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Alasti et al. (U. S. Patent Application No. 20030072326 A1) in view of Chao (U. S. Patent No. 6,487,213 B1), and in further teaches that view of Salandro (U. S. Patent No. 6,519,540 B1).

Regarding claim 43, Alasti teaches a hierarchical arbitration system for transferring information across a switch, the system comprising:

a switch including a first plurality of crossbars having a plurality of parallel routed inputs (120 in fig. 1)and a plurality of parallel routed outputs (130 in fig. 1) connected to

the switch inputs in response to the arbitration commands accepted on a control input (the outgoing lines from scheduler 140 in fig. 1);

an arbiter having an output connected to the switch control input to supply simultaneously arbitrated link commands for a plurality of links between the switch inputs and the switch outputs (scheduler in fig. 1 and fig. 2);

a queue assembler (121 in fig. 1) having a plurality of inputs to accept information packets having a plurality of cells ([0019])and addressing a plurality of outputs, and a control input to accept queue selection commands (the incoming lines from scheduler 140 to each input port 120 in fig. 1), the queue assembler grouping the information packets by switch output address ((fig. 1 and [0025]), queuing the information packets into a plurality of queues for each address grouping (121 in fig. 1 and [0025]), and supplying queues, selected in response to queue selection commands (the output lines from "scheduler in fig. 1), at a plurality of outputs connected to corresponding switch inputs (130 in fig. 1).

Alasti differs from the claimed invention in that Alasti does not specifically teaches that inputs accepting variably sized information packets and an arbiter having an output connected to the switch control input to supply simultaneously arbitrated link commands for a plurality of links between the switch inputs and the switch outputs for each crossbar. However, Chao teaches that the packets can be variable sized (col. 8 lines 21-24 and 27-33; fig. 19 and 20) and the crossbar switch has many crossbars(fig.20). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include accepting variably sized

information packets and switch has many crossbars, as taught by Chao in the assembly of Angle in order to accommodate different data packets and for high speed switching.

The modified assembly of Alasti and Chao differs from the claimed invention in that from the modified assembly does not specifically teach that the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links. However, Salandro teaches that the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links (col. 7 lines 11-15). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links, as taught by Salandro in the modified assembly of Alasti and Chao in order to prevent others from changing the signal path or establishing a signal path through the switch.

Regarding claim 44, Alasti further teaches the arbiter, for each crossbar, simultaneously arbitrates between each arbitrating switch output and a plurality of available switch inputs, having information packets to addressed to that switch output ([0021]).

Regarding claim 62, Alasti teaches a hierarchical arbitration system for transferring information across a switch, the system comprising:

a switch including a first plurality of crossbars having a plurality of parallel routed inputs (120 in fig. 1)and a plurality of parallel routed outputs (130 in fig. 1) connected to the switch inputs in response to the arbitration commands accepted on a control input (the outgoing lines from scheduler 140 in fig. 1);

an arbiter having an output connected to the switch control input to supply simultaneously arbitrated link commands for a plurality of links between the switch inputs and the switch outputs (scheduler in fig. 1 and fig. 2);

a queue assembler (121 in fig. 1) having a plurality of inputs to accept information packets having a plurality of cells ([0019])and addressing a plurality of outputs, and a control input to accept queue selection commands (the incoming lines from scheduler 140 to each input port 120 in fig. 1), the queue assembler grouping the information packets by switch output address ((fig. 1 and [0025]), queuing the information packets into a plurality of queues for each address grouping (121 in fig. 1 and [0025]), and supplying queues, selected in response to queue selection commands (the output lines from "scheduler in fig. 1), at a plurality of outputs connected to corresponding switch inputs (130 in fig. 1).

Alasti differs from the claimed invention in that Alasti does not specifically teaches that inputs accepting variably sized information packets and an arbiter having an output connected to the switch control input to supply simultaneously arbitrated link commands for a plurality of links between the switch inputs and the switch outputs for each crossbar. However, Chao teaches that the packets can be variable sized (col. 8 lines 21-24 and 27-33; fig. 19 and 20) and the crossbar switch has many crossbars

(fig.20). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include accepting variably sized information packets and switch has many crossbars, as taught by Chao in the assembly of Angle in order to accommodate different data packets and for high speed switching.

The modified assembly of Alasti and Chao differs from the claimed invention in that from the modified assembly does not specifically teach that the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links. However, Salandro teaches that the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links (col. 7 lines 11-15). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the switch locks the links between switch inputs and switch outputs, in response to commands from the arbiter, to transfer information packets across the links, as taught by Salandro in the modified assembly of Alasti and Chao in order to prevent others from changing the signal path or establishing a signal path through the switch.

9. Claims 45-47 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Alasti et al. (U. S. Patent Application No. 20030072326 A1) in view of Chao (U. S. Patent No. 6,487,213 B1) and Salandro (U. S. Patent No. 6,519,540 B1), and further in view of Krishna et al. (U. S. Patent Application No. 20010050916 A1).

Regarding claim 45, the modified assembly of Alasti, Chao and Salandro differs from the claimed invention in that the modified assembly does not specifically teach that the arbiter arbitrates between each arbitrating switch output and a plurality of available switch inputs by selecting the least recently used available switch input. However, Krishna teaches the arbiter arbitrates between each arbitrating switch output and a plurality of available switch inputs by selecting the least recently used available switch input ([0124] and TABLE 1 "picks the requesting input port with the oldest time stamp set along with the request"). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the arbiter arbitrates between each arbitrating switch output and a plurality of available switch inputs by selecting the least recently used available switch input, as taught by Krishna in the modified assembly of Alasti, Chao and Salandro in order to arbitrate effectively which input ports receives the grant from the output port.

Regarding claim 46, Alasti further teaches that the arbiter arbitrates between each arbitrating switch output and a plurality of available switch inputs, in a plurality of arbitration cycles for each crossbar (repeating processes in fig. 3).

Regarding claim 47, Alasti further teaches that the arbiter includes an available switch input priority list for each switch output; and, wherein the arbiter nominates switch inputs, for each arbitrating switch output, in response to the available switch input priority list ([0030] and [0031]).

Regarding claim 63, the modified assembly of Alasti, Chao and Salandro differs from the claimed invention in that the modified assembly does not specifically teach that the arbiter selects the least recently available queue, for each crossbar. However, Krishna teaches the arbiter selects the least recently available queue, for each crossbar ([0124] and TABLE 1 "picks the requesting input port with the oldest time stamp set along with the request"). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the arbiter arbitrates between each arbitrating switch output and a plurality of available switch inputs by selecting the least recently used available switch input, as taught by Krishna in the modified assembly of Alasti, Chao and Salandro in order to arbitrate effectively which input ports receives the grant from the output port.

10. Claim 65 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Alasti et al. (U. S. Patent Application No. 20030072326 A1) in view of Chao (U. S. Patent No. 6,487,213 B1) and Salandro (U. S. Patent No. 6,519,540 B1), and further in view of Fan et al. (U. S. Patent Application No. 20020122428 A1).

Regarding claim 65, Chao further teaches that accepting information packets having a ranked class of service (COS) (section 2.2.2 col. 7 lines 57-67 and col. 8 lines 1-18; section 5.1.6 col. 16 lines 52-57). The modified assembly of Alasti, Chao and Salandro differs from the claimed invention in that the modified assembly does not specifically teach that queue assembler accepts information packets having a ranked

class of service (COS), and queues the information packets by COS; and, wherein the arbiter selects a queue in response to COS of the information packet available for each crossbar. However, Fan teaches the queue assembler accepts information packets having a ranked class of service (COS), and queues the information packets by COS; and, wherein the arbiter selects a queue in response to COS of the information packet available for each crossbar ([0043] and [0045]). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include that the queue assembler accepts information packets having a ranked class of service (COS), and queues the information packets by COS; and, wherein the arbiter selects a queue in response to COS of the information packet available for each crossbar, as taught by Fan in the modified assembly in order to provide queuing structure for class Quality of Service (QoS).

11. Claims 48-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Alasti et al. (U. S. Patent Application No. 20030072326 A1) in view of Chao (U. S. Patent No. 6,487,213 B1), Salandro (U. S. Patent No. 6,519,540 B1) and Krishna et al. (U. S. Patent Application No. 20010050916 A1), and further in view of Angle et al. (U. S. Patent Application No. 20030174701 A1).

Regarding claim 48, the modified assembly of Alasti, Chao, Salandro and Krishna differs from the claimed invention in that the modified assembly does not specifically teach that the arbiter nominates the highest priority available switch input, for each arbitrating switch output, in a first arbitration cycle, and if the nominating switch

output is not accepted, the arbiter nominates successively lower priority available switch inputs in subsequent arbitration cycles. However, Angle teaches that the arbiter nominates the highest priority available switch input, for each arbitrating switch output, in a first arbitration cycle (fig. 7A and [0081]), and if the nominating switch output is not accepted, the arbiter nominates successively lower priority available switch inputs in subsequent arbitration cycles (fig. 7B and [0085]). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to include the arbiter nominates the highest priority available switch input, for each arbitrating switch output, in a first arbitration cycle, and if the nominating switch output is not accepted, the arbiter nominates successively lower priority available switch inputs in subsequent arbitration cycles, as taught by Angle in the modified assembly of Alasti, Chao, Salandro and Krishna in order to maximize the through put of the switch.

Regarding claim 49, Angle further teaches that the arbiter arbitrates between the nominating switch outputs in response to a switch input receiving multiple switch output nominations (fig. 7B and [0085]).

Regarding claim 50, Angle further teaches that the arbiter arbitrates between the nominating switch outputs by accepting the least recently available nominating switch output (fig. 7B and [0085]).

Regarding claim 51, Angle further teaches that the arbiter further includes a nominating switch output priority list for each available switch input ("priority indicator" for output ports in each input port in fig. 7B; and [0085]); and, wherein the arbiter accepts nominating switch outputs in response to the nominating switch output priority list (fig. 7B; and [0085]).

Regarding claim 52, Angle further teaches that the arbiter simultaneously accepts nominating switch outputs from the nominating switch output priority lists, for each switch input receiving a plurality of nominating switch outputs ("priority indicator" for output ports in each input port in fig. 7B; and [0085] and [0085]).

Regarding claim 53, Angle further teaches that the each available switch input priority list includes a sequential input pointer ("priority indicator" for input ports in each out port in fig. 7A; and [0081]), that, following the acceptance of a first nominating switch output by a first switch input, is incremented to a second switch input, next in sequence to the first switch input (fig. 7A and [0081]); and, wherein the arbiter nominates the available switch input closest in succession to the second switch input in subsequent arbitrations (fig. 7A; and [0081]).

Regarding claim 54, Angle further teaches that the input pointer is incremented in response to the acceptance of the first nominating switch output by a first switch input, in the first arbitration cycle only (fig. 6 step 650; fig. 7A and [0081]).

Regarding claim 55, Angle further teaches that the each nominating switch output priority list includes a sequential output pointer that ("priority indicator" for output ports in each input port in fig. 7B; and [0085]), following the acceptance of a nominating switch output, is incremented to a second switch output, next in sequence to the first switch output; and, wherein the arbiter accepts the nominating switch output closest in succession to second switch output in subsequent arbitrations (fig. 6 step 650; fig. 7B; and [0085]).

Regarding claim 56, Angle further teaches that the output pointer is incremented in response to the acceptance of the first nominating switch output by a first switch input, in the first arbitration cycle only (fig. 6 step 650).

Allowable Subject Matter

12. Claims 21-24, 27, 29-35, 57-61, 64 and 66-71 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lina Yang whose telephone number is (571)272-3151. The examiner can normally be reached Monday through Thursday between 8:00 a.m. and 7:00 p.m. eastern standard time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 517-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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